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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,476	09/21/2004	Teck Tiong Tan	DP-311441	5475

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HARTMAN & HARTMAN, P.C.
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EXAMINER

LIVEDALEN, BRIAN J

ART UNIT	PAPER NUMBER
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2878

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,476	TAN ET AL.	
	Examiner	Art Unit	
	Brian J. Livedalen	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to amendment filed 2/22/2007. Claims 1-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 6, 7, and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Nakayama et al. (6518656).

In regard to claim 1, Chen discloses (fig. 7) an electronic module having a housing (40) having an opening through which light enters the housing; a first substrate (20) coupled to the housing, the first substrate defining a window formed of a material that is at least semitransparent to light of a predetermined wavelength, the window being aligned with the housing so that light passing through the opening of the housing also passes through the window (column 2, lines 58-61, column 4, lines 15-25); a second substrate (50, 21) on a surface of the first substrate oppositely disposed from the housing, the second substrate comprising electrical conductors (21) and having an opening that is aligned with the housing so that light that passing through the housing and the window of the first substrate also passes unimpeded through the opening (column 3, lines 7-10, column 4, lines 5, 22-25); a chip (10) disposed on the second

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substrate so as to be located over the opening therein, the chip having at least one light-sensing element aligned for sensing light of the predetermined wavelength passing through the opening in the second substrate; electrically-conductive connections (fig. 1, 13) electrically connecting the light-sensing element to the electrical conductors on the second substrate (column 2, line 65 – column 3, line 2); an opaque layer (24) surrounding the opening of the second substrate and coinciding with an edge of the opening, the opaque layer preventing light from entering the module through the second substrate (column 3, lines 10-18). Chen fails to disclose a means for preventing light from entering the module between the chip and the second substrate. However, Nakayama discloses (fig. 11) an imager package with means (13) for preventing light from entering the module between the chip and a substrate (column 3, lines 61-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a means to prevent light from entering the module in order to eliminate false detection due to unwanted light.

In regard to claim 4, Chen discloses that the opaque layer is carried by and bonded to the second substrate (column 3, lines 7-14).

In regard to claims 6 and 7, Chen in view of Nakayama discloses in Nakayama that the means for preventing light from entering the module between the chip and the second substrate includes a body encasing the chip on the second substrate, the body being substantially opaque to infrared light (column 3, lines 61-67).

In regard to claims 9 and 10, Chen discloses (fig. 7) a means (40, 4) for preventing light from entering the module through the first substrate, wherein the means

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for preventing light from entering the module through the first substrate comprises a portion of the housing surrounding the first substrate.

In regard to claim 11, Chen in view of Nakayama discloses an electronic module as set forth above. Chen in view of Nakayama fails to disclose the second opening of the housing entirely accommodating the first substrate. However, Chen discloses in the prior art (fig. 10) a housing (8) surrounding a first substrate (91) (column 1, lines 44-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to surround the first substrate with the portion of the housing in order to better enclose the module and better protect the imager from outside light.

In regard to claims 12 and 13, Chen in view of Nakayama discloses an electronic module as set forth above. Chen in view of Nakayama fails to disclose the electronic module being mounted to a motherboard. However, Chen discloses in the prior art (fig. 10) attaching the electronic module to a motherboard (95), and second electrically-conducting connections (94) that physically attach the second substrate to the motherboard and electrically connect the light-sensing element to the motherboard (column 1, lines 44-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the electronic module to a motherboard in order for the module to function and communicate with a larger system. Chen in view of Nakayama further discloses a body encasing the chip between the second substrate and the motherboard, the body being substantially opaque to light.

Claims 3, 14, 15, 17, 18, and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Segawa et al. (2002/0057468) and in further view of Nakayama et al. (6518656).

In regard to claim 14, Chen discloses (fig. 7) an optical sensing module having: a housing (4, 40) formed of a material that is opaque to light of a predetermined wavelength, the housing having first and second openings through which light enters and exits the housing, respectively (column 4, lines 26-32); a lens assembly (not labeled) containing at least one lens and disposed in the housing so that light entering and exiting through the first and second openings of the housing pass through the lens (column 4, lines 15-22); a first substrate (20) that is at least semitransparent to light of the predetermined wavelength, the first substrate being coupled to the housing and defining a window aligned with the housing so that light passing through the first opening of the housing, the lens, and the second opening of the housing also passes through the window (column 2, lines 58-61); a flexible substrate (50, 21) bonded to a surface of the first substrate oppositely disposed from the housing, the flexible substrate having electrical conductors (21), the flexible substrate having an opening therein that is aligned with the second opening of the housing so that light that passes through the second opening of the housing and the window of the first substrate also passes through the opening (column 3, lines 7-10, column 4, lines 5, 22-25); a chip (10) disposed on the flexible substrate so as to be located over the opening therein, the chip having at least one light-sensing element aligned to sense light of the predetermined wavelength that has passed through the opening in the flexible substrate; solder

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connections (fig. 1, 13) physically attaching the chip to the flexible substrate and electrically connecting the light-sensing element to the electrical conductors on the flexible substrate, the solder connections being spaced apart to define gaps therebetween (column 2, line 65 – column 3, line 2); an opaque layer (24) on the flexible substrate, surrounding the opening of the flexible substrate, and coinciding with an edge of the opening, the opaque layer preventing light of the predetermined wavelength from entering the module through the flexible substrate and means (40, 41) for preventing light of the predetermined wavelength from entering the module through the first substrate (column 3, lines 10-18). Chen fails to disclose the electrical conductors in a material that is at least semitransparent to light of the predetermined wavelength. However, Segawa discloses (fig. 2) an imager package with a flexible substrate having conductors in a material that is at least semitransparent to light of a predetermined wavelength (page 2, paragraph 0031). It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the conductors in a semitransparent material in order to insulate the conductors to provide better electrical signals. Chen in view of Segawa fails to disclose a means for preventing light from entering the module between gaps in the solder connections. However, Nakayama discloses (fig. 11) an imager package with means (13) for preventing light from entering the module between gaps in the solder connections (column 3, lines 61-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a means to prevent light from entering the

module between gaps in the solder connections in order to eliminate false detection due to unwanted light.

In regard to claim 15, Chen in view of Segawa discloses (fig. 4) that the flexible substrate comprises a flat cable of an electrically-insulating material, and the electrical conductors comprise circuitry traces for the chip and other surface-mount components on the flexible substrate (column 4, lines 1-25).

In regard to claims 17 and 18, Chen in view of Nakayama discloses in Nakayama that the means for preventing light from entering the module between the chip and the second substrate includes a body encasing the chip on the second substrate, the body being substantially opaque to infrared light (column 3, lines 61-67).

In regard to claim 20, Chen discloses (fig. 1) the means for preventing light from entering the module through the first substrate comprises a portion of the housing defining the second opening thereof.

In regard to claim 21, Chen discloses (fig. 7) that the portion of the housing abuts and is bonded to the flexible substrate.

In regard to claim 22, Chen in view of Segawa and Nakayama discloses an electronic module as set forth above. Chen in view of Segawa and Nakayama fails to disclose the second opening of the housing entirely accommodating the first substrate. However, Chen discloses in the prior art (fig. 10) a housing (8) surrounding a first substrate (91) (column 1, lines 44-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to surround the first substrate with the

portion of the housing in order to better enclose the module and better protect the imager from outside light.

In regard to claims 23 and 24, Chen in view of Segawa and Nakayama discloses an electronic module as set forth above. Chen in view of Segawa and Nakayama fails to disclose the electronic module being mounted to a motherboard. However, Chen discloses in the prior art (fig. 10) attaching the electronic module to a motherboard (95), and second electrically-conducting connections (94) that physically attach the second substrate to the motherboard and electrically connect the light-sensing element to the motherboard (column 1, lines 44-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the electronic module to a motherboard in order for the module to function and communicate with a larger system. Chen in view of Segawa and Nakayama further discloses a body encasing the chip between the second substrate and the motherboard, the body being substantially opaque to light.

In regard to claim 3, Chen in view of Nakayama discloses an electronic module with a flexible substrate as set forth above. Chen in view of Nakayama fails to disclose that the electrical conductors in an insulating material. However, Segawa discloses (fig. 2) an imager package with a flexible substrate having conductors in an insulating material (page 2, paragraph 0031). It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the conductors in an insulating material in order to insulate the conductors to provide better electrical signals.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Nakayama et al. (6518656) as applied to claim 1, and in further view of Oxman et al. (6395124).

In regard to claim 2, Chen in view of Nakayama discloses an electronic module with a flexible substrate as set forth above. Chen in view of Nakayama fails to disclose laminating the flexible substrate to the first substrate. However, Oxman teaches using lamination to secure two substrates (column 20, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to laminate the substrates together in order to bond the substrates using a safe and low-temperature process (column 7, lines 1-20).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Nakayama et al. (6518656) as applied to claim 4, and in further view of Ono (2003/0214024) and in view of Oxman et al. (6395124).

In regard to claim 5, Chen in view of Nakayama discloses an electronic module with a flexible substrate with an opaque underlayer as set forth above. Chen in view of Nakayama fails to disclose the opaque layer being conductive. However, Ono discloses (fig. 1B) a light-shielding layer (7) that is made out of a conductive material (page 7, paragraph 0115). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a conductive material in order to maintain sufficient electrical connections between the conductors and the rest of the flexible substrate. Chen in view of Nakayama and Ono fails to disclose laminating the flexible substrate to

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the first substrate. However, Oxman teaches using lamination to secure two substrates (column 20, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to laminate the substrates together in order to bond the substrates using a safe and low-temperature process (column 7, lines 1-20).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Nakayama et al. (6518656) as applied to claim 6, and in further view of Sakurai (6765236).

In regard to claim 8, Chen discloses (fig. 1) that the electrically-conductive connections (13 left and right) are spaced apart on the chip to define gaps therebetween, the module further having an underfill material (12) that underfills the chip on the second substrate and fills the gaps between the electrically-conductive connections to promote reliability of the electrically-conductive connections, the body encasing the underfill material on the second substrate (column 2, lines 60-62). Chen in view of Nakayama fails to disclose the underfill also completely filling a gap between the chip and the first substrate. However, Sakurai teaches (fig. 3) completely filling a gap (34) between a first substrate (30) and a chip (10) (column 4, lines 66, 67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to completely fill the gap between the chip and the first substrate in order to control the amount of light that reaches the chip (column 5, lines 1-4).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Segawa et al. (2002/0057468) and Nakayama et al. (6518656) as applied to claim 4, and in further view of Ono (2003/0214024) and in view of Oxman et al. (6395124).

In regard to claim 16, Chen in view of Segawa and Nakayama discloses an electronic module with a flexible substrate with an opaque underlayer as set forth above. Chen in view of Segawa and Nakayama fails to disclose the opaque layer being conductive. However, Ono discloses (fig. 1B) a light-shielding layer (7) that is made out of a conductive material (page 7, paragraph 0115). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a conductive material in order to maintain sufficient electrical connections between the conductors and the rest of the flexible substrate. Chen in view of Segawa, Nakayama, and Ono fails to disclose laminating the flexible substrate to the first substrate. However, Oxman teaches using lamination to secure two substrates (column 20, lines 14-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to laminate the substrates together in order to bond the substrates using a safe and low-temperature process (column 7, lines 1-20).

Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6828543) in view of Segawa et al. (2002/0057468) and Nakayama et al. (6518656) as applied to claim 17, and in further view of Sakurai (6765236).

In regard to claim 19, Chen discloses (fig. 1) that the electrically-conductive connections (13 left and right) are spaced apart on the chip to define gaps therebetween, the module further having an underfill material (12) that underfills the chip on the second substrate and fills the gaps between the electrically-conductive connections to promote reliability of the electrically-conductive connections, the body encasing the underfill material on the second substrate (column 2, lines 60-62). Chen in view of Segawa and Nakayama fails to disclose the underfill also completely filling a gap between the chip and the first substrate. However, Sakurai teaches (fig. 3) completely filling a gap (34) between a first substrate (30) and a chip (10) (column 4, lines 66, 67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to completely fill the gap between the chip and the first substrate in order to control the amount of light that reaches the chip (column 5, lines 1-4).

Response to Arguments

Applicant's arguments with respect to claims 8, 11, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 2/22/2007 have been fully considered but they are not persuasive.

Applicant first argues that Chen fails to disclose the opaque layer (24) being carried by and bonded to the second substrate (21, 50). However, figure 7 clearly shows the opaque layer bonded to the bottom of 21 and the top of 50. Although the

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specification describes the opaque layer being bonded to 20, this fact does not preclude the bonding to 21 and 50 as demonstrated by the figures. The specification discloses the conduction interconnection circuit (21) formed on the bottom of the glass plate (column 3, lines 7-9). To be consistent with the figures, the opaque layer must be placed below 21.

Applicant next asserts that Chen fails to disclose the opaque layer preventing light from entering the module through the second substrate. Examiner pointed to 21 and 50 as the second substrate. Although the opaque layer does not prevent light from entering through 50, it does prevent light from entering through 21 as it completely covers the edges of 21. Therefore, Examiner maintains the present rejection.

Conclusion

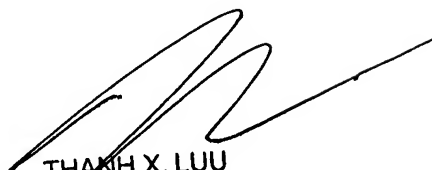
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Livedalen whose telephone number is (571) 272-2715. The examiner can normally be reached on 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



THANH X. LUU
PRIMARY EXAMINER

bjl